CLAIMS

1. A semiconductor device comprising: a first semiconductor chip and a second semiconductor chip stacked,

wherein said first semiconductor chip includes

a first electrode portion for connecting to an external electrode through wiring,

a second electrode portion having micro bumps for connecting a circuit in said second semiconductor chip to said first electrode portion, and

a third electrode portion having micro bumps for connecting a circuit block in said first semiconductor chip to the circuit in said second semiconductor chip; and

said second semiconductor chip includes

a fourth electrode portion having micro bumps for connecting to the second electrode portion in said first semiconductor chip, and

a fifth electrode portion having micro bumps for connecting to the third electrode portion in said first semiconductor chip.

2. The semiconductor device according to claim 1,

wherein the second electrode portion in said first semiconductor chip and the fourth electrode portion in said second semiconductor chip are arranged in the vicinity of a peripheral portion on each chip and,

the third electrode portion in said first semiconductor

chip and the fifth electrode portion in said second semiconductor chip are arranged in the vicinity of the center portion on each chip.

3. The semiconductor device according to claim 1,

wherein said first semiconductor chip includes a circuit block for memory, and

said second semiconductor chip includes a circuit block for control.

4. The semiconductor device according to claim 1,

wherein the micro bumps constituting said third and fifth electrode portions are arranged at least by the number corresponding to the number of bits of a memory which is included in said first semiconductor chip and in which the readout or writing is performed in parallel.